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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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7590

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EXAMINER

NGUYEN, MINH T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 07/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/921,561

Applicant(s)

KOMURA ET AL.

Examiner

Minh Nguyen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 May 2002.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All   b) ☐ Some \*   c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. Applicants' amendment filed on 5/15/02 has been received and entered in the case. The amendment and argument presented therein overcome the indefiniteness rejections and informality objections, and therefore, are withdrawn. New grounds of rejections necessitated by the amendment are set forth below. This action is FINAL.

### ***Claim Objections***

2. Claim 3 is objected to because of the following informalities: line 6, "output" should be changed to --input--; line 7, "input", second occurrence, should be changed to --output--.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 16-18, 26 and 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,521,540 to Marbot.

As per claim 1, Marbot discloses a delay circuit (Fig. 7) comprising:

a delay section having two or more predetermined delay stages (delay stages D1, D2, ..., D4), each predetermined delay stage adds a predetermined delay time to an input signal E0 (the first stage D1 adds a first predetermined delay time D1 to the input signal, the second stage D2 adds a second predetermined delay time D2 to the input signal, ...); and

selecting switch sections (U0, U1, ..., U4) for establishing a delay path (the path from E0 to Fk that outputs a delayed output signal) having the desired delay time, wherein

at least one of the selecting switch sections (U1, for example) comprises:

a buffer section (the combination of transistors P1 and N1 and resistors R1 and R1\*) for receiving delayed input signal E1 from one of the delay stages (the delay stage D1); and

a selecting section (transistors SW1\* and SW1) directly connected to the buffer section (transistor SW1\* is directly connected to resistor R1\*) for activating the buffer section to establish the delay path, and wherein

an output signal (at node Fk) from the delay path has the desired delay time.

As per claim 2, Marbot further discloses:

at least one of the predetermined delay stages (D1) is provided with an individual delayed output terminal E1 for outputting an individual delayed output signal (the signal at E1) having an individual predetermined delay time (the delay time caused by the delay stage D1); and wherein

at least one selecting switch section U1 is provided for each individual delayed output terminal E1 with an input terminal (the gates of P1, N1 is seen as the input terminal of the selecting switch section) of the buffer section (P1, N1, R1\*, R1) being connected to the individual delayed output terminal E1 (E1 connected to the gates of P1 and N1) and output terminals of the selecting switch sections being mutually joined (connected to line L).

As per claim 3, Marbot further discloses:

at least one predetermined delay stage D1 is provided with individual delayed input terminal E0 for inputting a signal (the signal at E0) to which the predetermined delay time is added, the rise delay time and fall delay time for the input signal of each of the predetermined delay stages in the Marbot circuit are substantial uniform because the Marbot circuit has the same structure of the recited delay circuit structure; and wherein

at least one selecting switch section U0 is provided for each individual delayed input terminal E0 with an input terminal of the selecting switch section being connected to the individual delayed input terminal E0 and the output terminals of the buffer sections being mutually joined (connected to line L through the selecting section).

As per claim 16, the recited connections of the delay stages are shown in Fig. 7.

As per claim 17, this claim is rejected for the same reason noted in claim 16.

As per claim 18, since the recited predetermined delay stages do not have any structural different from the Marbot's predetermined delay stages, they should output the same results, i.e., the rise delay time and fall delay time for an input signal are also balanced so as to be substantial uniform.

As per claim 26, this claim is rejected for the same reason noted in claim 1.

As per claim 29, this claim is merely a method to operate the delay circuit having elements and connections as discussed in claim 1 above, since Marbot teaches the circuit, he inherently teaches the method wherein the recited delay step is performed by delays D1, ..., D4; the recited output step is the result signals at output nodes of the delay stages D1, ..., D4; and the recited selecting step is performed by control signals (A0, ..., A4) via switches (SW0, ..., SW4).

As per claim 30, the recited required power reads on the power supply VDD.

As per claim 31, this claim is rejected for the same reason noted in claim 18.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-15, 19-25 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,521,540 to Marbot.

As per claim 4, Marbot teaches a delay circuit as discussed in claim 1 above, and further, the recited first transistor in the buffer section reads on transistors P1 having a gate terminal set as an input terminal, the recited second transistor in the selecting section reads on transistors SW\*1 whose gate terminal a control signal A1 for establishing the delay path in the delay section is input, and the first and second transistors are connected in series through the variable resistor R1\* between the output terminal (line L) and a first power supply voltage VDD.

Marbot does not explicitly teach that the first and second transistors are connected directly in series as called for in the claim.

In column 8, lines 51-64, Marbot teaches that the purpose of the variable resistors R1 and R1\* is for controlling the rise and fall time of the output signals by controlling the resistance of these variable resistors, i.e., the time for the output signal to rise from 0 to VDD or to fall from VDD to 0 is controlled by the variable resistors R1 and R1\*.

It would have been obvious to one skilled in the art at the time of the invention was made to remove the variable resistors R1 and R1\* in the selecting switch section of the Marbot's delay circuit for applications which do not require the control of the rise and fall times of the output signals.

The motivation/suggestion for doing so would have been obvious since by removing these variable resistors R1 and R1\* in the Marbot delay circuit, less components are needed, and therefore, the cost to implement the Marbot delay circuit is reduced.

Therefore, it would have been obvious to remove the variable resistors R1 and R1\* in the Marbot's delay circuit to obtain the invention specified in the claim.

As per claim 5, the combination discussed in claim 4 above discloses the second transistor is connected between the first transistor and the output terminal (line L) and these transistors are in series but it does not explicitly disclose that these transistors can be interchanged, i.e., the first transistor is connected between the second transistor and the output terminal (line L) as called for in the claim.

However, it is notoriously well-known to a person skilled in the art that the position of these transistors can be interchanged since in either location they perform the same function and output the same results. Since they are art recognized equivalent, during assembly process, the worker can perform the rearrangement so that the layout yields the most convenient way to receive the control signals and input signals and /or further minimize the electromagnetic interference problems (EMI).

It would have been obvious to one skilled in the art at the time of the invention was made to provide the second transistors (SW\*0, ..., SW\*4) at the first power supply side VDD and the first transistors (P0, ..., P4) at the output side in the Marbot's delay circuit.

The motivation/suggestion for doing so would have been obvious for the reasons discussed herein above.

Therefore, it would have been obvious to interchanged to locations of the first and second transistors in the Marbot delay circuit to obtain the invention specified in the claim.

As per claim 6, as shown in Fig. 7, the first transistors (P0, ..., P4) are provided at the first power supply side VDD and the second transistors (SW\*0, ..., SW\*4) are provided at the output terminal side of the selecting switch sections.

As per claim 7, the recited third transistors read on transistors (N0, ..., N4), the recited fourth transistors read on transistors (SW0, ..., SW4), the recited second power supply voltage reads on the supply voltage VSS. These elements are connected as recited.

As per claim 8, Marbot teaches a delay circuit as discussed in claim 7 above wherein the first transistors are provided at the first power supply side VDD, the second and fourth transistors are provided at the output terminal side (line L), and the third transistors are provided at the second power supply side VSS but he does not explicitly teach that the second transistors are provided at the first power supply side VDD, the first and third transistors are provided at the output terminal side (line L), and the fourth transistors are provided at the second power supply side VSS as called for in the claim.

However, the recited arrangement is an obvious alternation of the arrangement shown in Fig. 7 of the Marbot reference, and one skilled in the art would be motivated to rearrange the



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transistors in the Marbot circuit to be the same as the one recited in the claim for the reasons and motivations discussed in claim 5 above.

As per claim 9, Fig. 7 shows the first, second, third and fourth transistors are connected as recited in the claim.

As per claim 10, the first power supply voltage VDD is the recited power supply voltage potential, and Fig. 8 shows the first and second transistors are PMOS transistors.

As per claim 13, the second power supply voltage VSS is the recited ground supply voltage potential, and Fig. 8 shows the third and fourth transistors are NMOS transistors.

As per claims 11 and 12, these claims are merely the same as claims 10 and 13, respectively when the names of the first and second transistors are interchanged with the names of the third and fourth transistors and the names of the first and second power supply voltages are interchanged, and therefore, they are rejected for the same reasons as discussed in claim 10 and 13.

As per claim 14, Marbot teaches a delay circuit as discussed in claim 4 above wherein the first transistors which are functioned as buffers are provided at the first power supply side VDD and the second transistors which are functioned as switches are provided at the output terminal side (line L) but he does not explicitly disclose that the drive capacity of the second transistors are larger than the drive capacity of the first transistors as called for in the claim.

However, it is notoriously well-known to a person skilled in the art that a transistor which is functioned as a switch introduces a delay when a signal passes through, and by increasing the drive capacity of the transistor, the delay caused by the transistor is reduced.

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It would have been obvious to one skilled in the art at the time of the invention was made to use a larger drive capacity of the second transistors than the drive capacity of the first transistors in the Marbot delay circuit.

The motivation/suggestion for doing so would have been to improve the accuracy of the Marbot delay circuit by eliminating the unaccounted delays by the switches.

Therefore, it would have been obvious to use the second transistors having drive capacity larger than the drive capacity of the first transistors in the Marbot delay circuit to obtain the invention specified in the claim.

As per claim 15, this claim is rejected for the same reason and motivation as discussed in claim 14.

As per claim 19, Marbot discloses the delay circuit which includes predetermined delay stages D1, ..., D4 as discussed in claim 18 above but he does not explicitly disclose that each of the delay stages is implemented using even basis units connected in series as called for in the claim.

The examiner takes Official Notice that it is old and well-known in the art to use inverters connected in series as a delay stage, and each of the inverters is counted as a basis unit delay, two inverters can be connected in series to implement a delay stage in a delay circuit so that the rise and fall times of an input signal are balanced.

It would have been obvious to one skilled in the art at the time of the invention was made to use two inverters connected in series to implement each of the Marbot's delay stages D1, ..., D4.

The motivation/suggestion for doing so would have to obtain a balanced rise and fall time of the output signal when the signal is delayed by the Marbot's delay circuit.

Therefore, it would have been obvious to use two inverters to implement each of the Marbot delay stages to obtain the invention specified in the claim.

As per claim 20, the modification discussed in claim 19 clearly discloses the logic inversion sections are inverter gates.

As per claim 21, this claim is rejected for the same reasons noted in claim 19. Regarding the limitation that the rise delay time and fall delay time of an input signal are different, this limitation is met when the delay stage is implemented using odd number of inverters.

As per claim 24, Marbot discloses the delay circuit which includes predetermined delay stages D1, ..., D4 as discussed in claim 16 above but he does not explicitly disclose that each of the delay stages having the same structure.

The examiner takes Official Notice that using the same structure to implement each of the delay stages has the advantage of cost reducing since they are able to mass production.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Marbot delay stages using the same structure for the advantage of minimizing the cost.

As per claims 22 and 23, the combination discussed in claim 21 above discloses the delay circuit includes predetermined delay stages D1, ..., D4 wherein each of the delay stage is implemented using two inverters connected in series but he does not explicitly disclose that each of the delay stages is implemented using NAND gates to function as inverters by connecting one of its input terminal to VDD as called for in claim 22 or each of the delay stages is implemented

using NOR gates to function as inverters by connecting one of its input terminal to ground as called for in claim 23.

The examiner takes Official Notice that an NAND gate with one of its input terminals connected to VDD or a NOR gate with one of its input terminals connected to ground is art recognized equivalent to an inverter since it is functioned as an inverter.

It would have been obvious to replace the inverters used to implement the delay stages in the combination discussed in claim 21 with NAND gates or NOR gates.

The suggestion/motivation for doing so would have been obvious since during the assembly process of the Marbot circuit, a worker would be motivated to replace the inverter in the Marbot delay stage by a NAND gate or NOR gate when the inverter is not readily available, and therefore, time for waiting the parts is saved.

Therefore, it would have been obvious to replace the inverters in the delay stage of the Marbot circuit by NOR gates as called for in claim 23 or by NAND gates as called for in claim 22 to obtain the invention specified in the claims.

As per claim 25, as shown in Fig. 8, more controls (K0, K\*0) and more transistors (the transistors which receives control signals K0, K\*0) are added in series.

As per claims 27-28, these claims are rejected for the same reasons noted in claims 4 and 18, respectively.

### ***Response to Arguments***

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

It is further noted that since the Applicants do not traverse the Examiner's assertion of Official Notices taken in the previous Office Action, the common knowledge and well-known in the art statements are taken to be admitted prior art.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

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organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

*M*

MN  
June 26, 2002

*Kenneth B. Wells*  
Kenneth B. Wells  
Primary Examiner